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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,949	GREGORI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. All of claims 11-28 are examined in the current Office Action. The Examiner would like to warn the Applicant that since newly added claims16-25 appear to contain all of the language as cancelled claims 1-10, if a continuation is filed with claims 1-10, a non-statutory double-patenting rejection requiring a terminal disclaimer may be required.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it exceeds 150 words and because it uses form and legal phraseology such as: “said” and “aforesaid”. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: Claim 1 recites, "an error control method for multilevel memory cells operating with a variable number of storage levels". Nowhere in the specification does the Applicant teach the steps of claims 16-24 as part of "an error control method for multilevel memory cells operating with a variable number of storage levels".

Appropriate correction is required.

Claim Objections

3. Claim15 is objected to because of the following informalities: "writ" in line 11 appears to be a typo. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 16-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites, "an error control method for multilevel memory cells operating with a variable number of storage levels". Nowhere in the specification does the Applicant teach the steps of claims 16-24 as part of "an error control method for

multilevel memory cells operating with a variable number of storage levels". The Encoder 132 uses a single error correction code once it is designed. Claims 16-24 are method steps for designing an error correction code and are not part of "an error control method for multilevel memory cells operating with a variable number of storage levels"

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 16-24 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between "an error control method for multilevel memory cells operating with a variable number of storage levels" in claim 1 and the method steps for designing an error correction code in claims 16-24.

Claims 16-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Symbols such as b, a_1, a_2,... are undefined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 11-15 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okita; Shigeru (US 6378104 B1) in view of Choi; Byeng-Sun (US 6233717 B1).

35 U.S.C. 103(a) rejection of claims 11 and 26.

Okita teaches an error control method, the method comprising: receiving a first information word having k input symbols each in a first base (Input Transformation Circuits 116 in Figure 1 of Okita is a device for receiving a first information word having k input symbols each in a first base); converting the first information word into a second base by converting the input symbols into input symbols in the second base (Input Transformation Circuits 116 in Figure 1 of Okita is a device for converting the first

information word into a second base by converting the input symbols into input symbols in the second base); and encoding the converted first information word into a first codeword having k+n coded symbols in the second base (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for encoding the converted first information word into a first codeword having k+n coded symbols in the second base).

However Okita does not explicitly teach the specific use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels.

Choi, in an analogous art, teaches writing the first codeword into multilevel memory cells operating with a variable number of storage levels (see Fig. 1 and the Abstract in Choi). One of ordinary skill in the art at the time the invention was made would have been highly motivated to use the transformation device in Okita for data streams or coded data streams existing in different formats from a coding or decoding device (col. 3, lines 52-64, Okita).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita with the teachings of Choi by including use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels would have provided the opportunity to use coding or decoding devices operating in a different basis from a data stream or a coded data stream (col. 3, lines 52-64, Okita).

35 U.S.C. 103(a) rejection of claims 12 and 27.

Okita and Choi teach receiving a second information word having k input symbols each in the second base (Input Transformation Circuits 116 in Figure 1 of Okita is a device capable of receiving a second information word having k input symbols each in the second base); encoding the second information word into a second codeword having k+n coded symbols in the second base (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for encoding the second information word into a second codeword having k+n coded symbols in the second base; Note: if the second codeword is already in the base used by the RS Coding/Decoding Core Unit 112, Input Transformation Circuits 116b-116x are bypassed); writing the second codeword into the multilevel memory cells (see Fig. 1 and the Abstract in Choi).

35 U.S.C. 103(a) rejection of claims 13 and 28.

Okita and Choi teach reading from the multilevel memory cells the first codeword (see Fig. 1 and the Abstract in Choi); decoding the first codeword into an estimated word having k estimated symbols in the second base (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for decoding the first codeword into an estimated word having k estimated symbols in the second base); and converting the estimated word into the first base by converting the estimated symbols into estimated symbols in the first base (Output Transformation Circuits 119 in Figure 1 of Okita is a device for

converting the estimated word into the first base by converting the estimated symbols into estimated symbols in the first base).

35 U.S.C. 103(a) rejection of claim 14.

Okita teaches decoding the first codeword into an estimated word having k estimated symbols in the second base (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for decoding the first codeword into an estimated word having k estimated symbols in the second base); and converting the estimated word into the first base by converting the estimated symbols into estimated symbols in the first base (Output Transformation Circuits 119 in Figure 1 of Okita is a device for converting the estimated word into the first base by converting the estimated symbols into estimated symbols in the first base).

However Okita does not explicitly teach the specific use of reading from the multilevel memory cells the first codeword.

Choi, in an analogous art, teaches use of reading from the multilevel memory cells the first codeword (see Fig. 1 and the Abstract in Choi). One of ordinary skill in the art at the time the invention was made would have been highly motivated to use the transformation device in Okita for data streams or coded data streams existing in different formats from a coding or decoding device (col. 3, lines 52-64, Okita).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita with the teachings of Choi by including use of reading from the multilevel memory cells the first codeword. This modification would

have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of reading from the multilevel memory cells the first codeword would have provided the opportunity to use coding or decoding devices operating in a different basis from a data stream or a coded data stream (col. 3, lines 52-64, Okita).

35 U.S.C. 103(a) rejection of claim 15.

Okita teaches an input transcoder having a word input that receives an information word having k input symbols each in the first base (Input Transformation Circuits 116 in Figure 1 of Okita is a device for receiving a first information word having k input symbols each in a first base), a control input that receives a control signal indicating whether the memory matrix is operating according to the first base or the second base (Switch 118 in Figure 1 of Okita is a control input that receives a control signal indicating whether the memory matrix is operating according to the first base or the second base), and an output that outputs a converted information word in the second base (Switch 118 in Figure 1 of Okita is an output that outputs a converted information word in the second base); an encoder coupled to the output of the input transcoder and structured to encode the converted infonnation word into a codeword having k + n coded symbols in the second base (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for encoding the converted first information word into a first codeword having k+n coded symbols in the second base).

However Okita does not explicitly teach the specific use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels.

Choi, in an analogous art, teaches writing the first codeword into multilevel memory cells operating with a variable number of storage levels (see Fig. 1 and the Abstract in Choi). One of ordinary skill in the art at the time the invention was made would have been highly motivated to use the transformation device in Okita for data streams or coded data streams existing in different formats from a coding or decoding device (col. 3, lines 52-64, Okita).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita with the teachings of Choi by including use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of writing the first codeword into multilevel memory cells operating with a variable number of storage levels would have provided the opportunity to use coding or decoding devices operating in a different basis from a data stream or a coded data stream (col. 3, lines 52-64, Okita).

35 U.S.C. 103(a) rejection of claim 25.

Okita and Choi teach decoding a word read in said memory, using said first codeword (RS Coding/Decoding Core Unit 112 in Figure 1 of Okita is a device for decoding a word read in said memory, using said first codeword); and converting, symbol by symbol, said

decoded word from the second base to the first base (Output Transformation Circuits 119 in Figure 1 of Okita is a device for converting, symbol by symbol, said decoded word from the second base to the first base).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133